WHAT IS CLAIMED IS:

1. A video codec system which is implemented in a processor independent from a host system and comprises an encoder for encoding video data input through a video input apparatus, and a decoder for decoding the encoded data sent from the host system and outputting the decoded data to a video output apparatus, the video codec system comprising:

an encoder buffer for temporarily storing a bit stream encoded in the encoder, before the bit stream is sent to the host system;

a decoder buffer for temporarily storing the encoded data sent from the host system;

a task status register for writing task statuses of the encoder, decoder, encoder buffer and decoder buffer, in the form of predetermined bits;

a command identification register for writing a command to be executed by the encoder and the decoder; and

an interface and control manager for parsing a command sent from the host system, writing the command in the command identification register, checking each task through the task status register, and then controlling the encoder and the decoder through the command identification register.

2. The video codec system of claim 1, wherein the encoder buffer and decoder buffer include bits in which their respective statuses are shown as any one of empty level, full level, half level, and user-defined level.

3. The video codec system of claim 1, wherein the command identification register includes at least a bit for indicating that one or more commands to be executed by the encoder and decoder exist, bits for indicating the number of commands to be executed, and a bit for indicating that the encoder and decoder have fetched all the commands.

4. A data processing method for processing data between a video codec system, which is implemented in a processor independent from a host system, and the host system, the data processing method comprising the steps of:

(a) determining whether data input from an external host system is a control command or transmitting data;

(b) checking whether or not a set of commands is completed when the input data is a control command, and accumulating the control command when the set of commands is not completed, and then performing the step (a), and writing commands to be executed in pre-assigned bits of a command identification register when the set of commands is completed;

(c) making a first pre-assigned bit of the command identification register indicate that commands to be executed by the encoder and/or decoder exist; and

(d) checking the content indicated in the step (c) and then fetching the command written in the step (b) in the encoder and/or the decoder.

5. The data processing method of claim 4, after the step (d) further comprising the step of:

(e) performing a command, and making a second pre-assigned bit of the command identification register indicate that all commands have been fetched in the encoder and/or the decoder.

6. An encoding/decoding control method in a video codec system which is implemented in a processor independent from a host system, the encoding/decoding control method comprising the steps of:

(a) resetting pre-assigned bits of a task status register in the video codec system so that an encoder and/or decoder can operate when a start command is input from the host system;

(b) determining whether or not to perform encoding and/or decoding, by checking a reset of the task status register in the encoder and/or decoder;

(c) making pre-assigned bits of the task status register indicate buffer statuses of an encoder buffer and a decoder buffer; and

(d) checking the buffer statuses of the encoder buffer and the decoder buffer written in the task status register, and then controlling tasks of the encoder and the decoder.